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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/905,584	07/13/2001	Kelly T. Hurley	2000-0133.00/US	4272

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EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/905,584	HURLEY, KELLY T.	
	Examin r	Art Unit	
	Kevin Quinto	2826	

-- Th MAILING DATE of this communication app ars on the cov r she t with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *13 July 2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishii (JP 64-13771).

3. In reference to claims 1, 3, and 13, Ishii (JP 64-13771) discloses a similar method of forming a floating gate. Figures 4(a)-(d) illustrate a tunnel oxide (11, 12) with openings that expose the underlying silicon (1). An epitaxial layer is formed over the tunnel oxide (11, 12) by using the exposed silicon as a seeding source (abstract).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii (JP 64-13771) in view of Jastrzebski et al. (USPN 4,615,762) and further in view of Fisher (USPN 4,272,882).

6. In reference to claim 2, Ishii does not disclose depositing epitaxial silicon on the exposed silicon substrate. However this method of depositing silicon is well known in the art. Jastrzebski (USPN 4,615,762) discloses that depositing epitaxial silicon on exposed silicon or epitaxial lateral overgrowth leads to a high quality single crystal silicon. Fisher (USPN 4,272,882) discloses that high quality silicon crystal leads to the benefit of greater reliability (column 1, lines 14-16). Therefore in view of Jastrzebski and Fisher, it would be obvious to deposit epitaxial silicon as a means of forming the floating gate.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii (JP 64-13771) in view of Murai (USPN 5,243,559) and further in view of Koyama et al. (USPN 5,981,366) and further in view of Sheu et al. (USPN 6,350,654 B1).

8. In reference to claim 4, Ishii does not disclose doping the floating gate. However doping the floating gate is well known in the art. Murai (USPN 5,243,559) discloses that doping the floating gate reduces its resistivity (column 4, lines 37-42). The desire for a low resistance floating gate is also well known in the art. Koyama et al. (USPN 5,981,366, hereinafter referred to as the "Koyama" reference) discloses that a low resistance floating gate leads to a faster response time (column 1, lines 27-35). Furthermore Sheu et al. (USPN 6,350,654 B1, hereinafter referred to as the "Sheu" reference) discloses that faster memory devices are a known goal in the art (column 1, lines 15-35). Therefore in view of Koyama, Sheu, and Murai, it would be obvious to dope the floating gate in order to enhance the speed of the device.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii (JP 64-13771) in view of Murai (USPN 5,243,559) and further in view of Koyama et al. (USPN 5,981,366) and further in view of Sheu et al. (USPN 6,350,654 B1) as applied to claim 4 above and further in view of Wang (USPN 6,410,090 B1) and further in view of Lo et al. (USPN 6,507,098 B1).

10. In reference to claim 5, Ishii does not disclose doping the floating gate by way of insitu doping. However insitu doping is well known in the art. Wang (USPN 6,410,090 B1) discloses an insitu doping process which has the benefit of reducing the cost of fabrication (column 3, lines 22-27). Lo et al. (USPN 6,507,098 B1, hereinafter referred to as the "Lo" reference) discloses that low cost fabrication is a well known goal in the semiconductor art (column 1, lines 12-14). In view of Wang and Lo, it would therefore be obvious to utilize insitu doping as the means of doping the floating gate.

11. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii (JP 64-13771) in view of Murai (USPN 5,243,559) and further in view of Koyama et al. (USPN 5,981,366) and further in view of Sheu et al. (USPN 6,350,654 B1) as applied to claim 4 above and further in view of Shopbell (USPN 6,055,460) and further in view of Farber et al. (USPN 6,187,684 B1).

12. In reference to claim 6, Ishii does not disclose doping the floating gate by way of ion implantation. However ion implantation is well known in the art. Shopbell (USPN 6,055,460) discloses that ion implantation doping has the benefit of taking place in a clean environment (column 6, lines 35-38). Farber et al. (USPN 6,187,684 B1, hereinafter referred to as the "Farber" reference) discloses that fabrication in a clean

environment is desired in the semiconductor art (column 2, lines 23-26). In view of Shopbell and Farber, it would therefore be obvious to utilize ion implantation as the means of doping the floating gate.

13. Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii (JP 64-13771) in view of Noda et al. (USPN 5,068,697) and further in view of Sheu (USPN 6,350,654 B1).

14. In reference to claims 7 and 9, Ishii (JP 64-13771) discloses a similar method of forming a flash memory. Figures 1,2, 4(a)-(d) illustrate a tunnel oxide (11, 12) with openings that expose the underlying silicon (1). An epitaxial layer is formed over the tunnel oxide (11, 12) by using the exposed silicon as a seeding source (abstract). An inner-dielectric layer (not labeled) is formed over the epitaxial layer. A polysilicon layer (24) is formed over the inner-dielectric layer. Together the polysilicon layer (24), the inner-dielectric layer, and the epitaxial layer form a transistor gate. It is understood that a plurality of gates are formed. Source and drain electrodes (5,4) are formed on opposing sides of the transistor gate. Ishii does not disclose forming a silicide on top of the polysilicon control gate (thereby forming a polycide). However the use of polycide on control gates is well known in the art. Noda et al. (USPN 5,068,697, hereinafter referred to as the "Noda" reference) discloses that control gates made of polycide leads to a faster non-volatile memory due to its low resistance qualities (column 2, lines 63-68 and column 3, lines 1-6). Furthermore Sheu (USPN 6,350,654 B1) discloses that faster memory devices are a known goal in the art (column 1, lines 15-35). In view of Noda

and Sheu, it would therefore be obvious to implement a polycide material as the control gate in the device of Ishii in order to attain this benefit.

15. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii (JP 64-13771) in view of Noda et al. (USPN 5,068,697) and further in view of Sheu et al. (USPN 6,350,654 B1) as applied to claim 7 above, and further in view of Jastrzebski et al. (USPN 4,615,762) and further in view of Fisher (USPN 4,272,882).

16. In reference to claim 8, neither Ishii nor Noda disclose depositing epitaxial silicon on the exposed silicon substrate. However this method of depositing silicon is well known in the art. Jastrzebski (USPN 4,615,762) discloses that depositing epitaxial silicon on exposed silicon or epitaxial lateral overgrowth leads to a high quality single crystal silicon. Fisher (USPN 4,272,882) discloses that high quality silicon crystal leads to the benefit of greater reliability (column 1, lines 14-16). Therefore in view of Jastrzebski and Fisher, it would be obvious to deposit epitaxial silicon as a means of forming the floating gate.

17. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii (JP 64-13771) in view of Noda et al. (USPN 5,068,697) and further in view of Sheu et al. (USPN 6,350,654 B1) as applied to claim 7 above and further in view of Murai (USPN 5,243,559) and further in view of Koyama et al. (USPN 5,981,366) and further in view of Sheu et al. (USPN 6,350,654 B1).

18. In reference to claim 10, Ishii does not disclose doping the floating gate. However doping the floating gate is well known in the art. Murai (USPN 5,243,559) discloses that doping the floating gate reduces its resistivity (column 4, lines 37-42).

The desire for a low resistance floating gate is also well known in the art. Koyama (USPN 5,981,366) discloses that a low resistance floating gate leads to a faster response time (column 1, lines 27-35). Furthermore Sheu (USPN 6,350,654 B1) discloses that faster memory devices are a known goal in the art (column 1, lines 15-35). Therefore in view of Koyama, Sheu, and Murai, it would be obvious to dope the floating gate in order to enhance the speed of the device.

19. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii (JP 64-13771) in view of Noda et al. (USPN 5,068,697) and further in view of Sheu et al. (USPN 6,350,654 B1) and further in view of Murai (USPN 5,243,559) and further in view of Koyama et al. (USPN 5,981,366) and further in view of Sheu et al. (USPN 6,350,654 B1) as applied to claim 10 above, and further in view of Wang (USPN 6,410,090 B1) and further in view of Lo et al. (USPN 6,507,098 B1).

20. In reference to claim 11, Ishii does not disclose doping the floating gate by way of insitu doping. However insitu doping is well known in the art. Wang (USPN 6,410,090 B1) discloses an insitu doping process which has the benefit of reducing the cost of fabrication (column 3, lines 22-27). Lo (USPN 6,507,098 B1) discloses that low cost fabrication is a well known goal in the semiconductor art (column 1, lines 12-14). In view of Wang and Lo, it would therefore be obvious to utilize insitu doping as the means of doping the floating gate.

21. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii (JP 64-13771) in view of Noda et al. (USPN 5,068,697) and further in view of Sheu et al. (USPN 6,350,654 B1) and further in view of Murai (USPN 5,243,559) and further in view

of Koyama et al. (USPN 5,981,366) and further in view of Sheu et al. (USPN 6,350,654 B1) as applied to claim 10 above, and further in view of Shopbell (USPN 6,055,460) and further in view of Farber et al. (USPN 6,187,684 B1).

22. In reference to claim 12, Ishii does not disclose doping the floating gate by way of ion implantation. However ion implantation is well known in the art. Shopbell (USPN 6,055,460) discloses that ion implantation doping has the benefit of taking place in a clean environment (column 6, lines 35-38). Farber (USPN 6,187,684 B1) discloses that fabrication in a clean environment is desired in the semiconductor art (column 2, lines 23-26). In view of Shopbell and Farber, it would therefore be obvious to utilize ion implantation as the means of doping the floating gate.

23. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii (JP 64-13771) in view of Murai (USPN 5,243,559) and further in view of Koyama et al. (USPN 5,981,366) and further in view of Sheu et al. (USPN 6,350,654 B1).

24. In reference to claim 14, Ishii does not disclose doping the floating gate with conductive ions. However doping the floating gate is well known in the art. Murai (USPN 5,243,559) discloses that doping the floating gate reduces its resistivity (column 4, lines 37-42). The desire for a low resistance floating gate is also well known in the art. Koyama (USPN 5,981,366) discloses that a low resistance floating gate leads to a faster response time (column 1, lines 27-35). Furthermore Sheu (USPN 6,350,654 B1) discloses that faster memory devices are a known goal in the art (column 1, lines 15-35). Therefore in view of Koyama, Sheu, and Murai, it would be obvious to dope the floating gate in order to enhance the speed of the device.

25. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii (JP 64-13771) in view of Noda et al. (USPN 5,068,697) and further in view of Sheu et al. (USPN 6,350,654 B1).

26. In reference to claim 15, Ishii (JP 64-13771) discloses a similar flash memory device. Figures 1,2, 4(a)-(d) illustrate a tunnel oxide (11, 12) with openings that expose the underlying silicon (1). An epitaxial layer is formed over the tunnel oxide (11, 12) by using the exposed silicon as a seeding source (abstract). An inner-dielectric layer (not labeled) is formed over the epitaxial layer. A polysilicon layer (24) is formed over the inner-dielectric layer. Together the polysilicon layer (24), the inner-dielectric layer, and the epitaxial layer form a transistor gate. It is understood that a plurality of gates are formed. Source and drain electrodes (5,4) are formed on opposing sides of the transistor gate. Ishii does not disclose forming a silicide on top of the polysilicon control gate (thereby forming a polycide). However the use of polycide on control gates is well known in the art. Noda (USPN 5,068,697) discloses that control gates made of polycide lead to a faster non-volatile memory due to its low resistance qualities (column 2, lines 63-68 and column 3, lines 1-6). Furthermore Sheu (USPN 6,350,654 B1) discloses that faster memory devices are a known goal in the art (column 1, lines 15-35). In view of Noda and Sheu, it would therefore be obvious to implement a polycide material as the control gate in the device of Ishii in order to attain this benefit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

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